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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LUU, PHO M	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 04/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/796,111	KLEIN A. DEAN	
	Examiner	Art Unit	
	Pho M. Luu	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *Amendment filed on 01/18/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-85* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-61,69-73 and 81-85* is/are allowed.

6)☒ Claim(s) *1-8,62-65 and 74-77* is/are rejected.

7)☒ Claim(s) *9-11,66-68 and 78-80* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search History*.

Amendment

1. Acknowledgment is made of applicant's Amendment, filed 18 January 2006. The changes and remarks disclosed therein were considered.

2. Claims 1-85 are pending in the application.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-8, 62-65 and 74-77 are rejected under 35 U.S.C. 102(b) as being anticipated by Takata et al. (US. 5,777,921).

Regarding claim 1, Takata et al discloses in figure 1, a memory refresh circuit comprising:

a control circuit (**main control circuit 9, figure 1**) for conducting a memory refresh operation (**by using the refresh control circuit 10, figure 1**) for monitoring a memory device (**memory array 1, figure 1**) and for indicating when the refresh operation is complete (**the refresh control circuit 10 for refresh the memory cell by applying a positive and negative electric field for causing the states of memory cell array 1 to transit at least one completed; also see column 9, lines 18-23**) based on the monitoring of the memory device (**main control circuit 9 coupled to**

memory array 1 through refresh control circuit 10 for refreshing individual memory cells MC array 1, also see column 9, lines 14-27).

With respect to claim 2, Takata et al discloses in figures 1 and 6, the refresh circuit (**refresh circuit 10, figure 1**) includes a refresh counter (**refresh counters 10a, 10b, figure 6, see column 11, lines 24-27**).

With respect to claim 3, Takata et al discloses in figures 1 and 6, the refresh circuit (**refresh circuit 10, figure 1**) comprises a refresh complete circuit (**the refresh circuit 10 including a first counter 10a corresponding to the memory cell MC when data DQ access at the HIGH level and a second counter 10b corresponding to the memory cell MC when data DQ access at the LOW level in figure 6; also see column 12, lines 13-21**) for indicating when the refresh operation is complete (**the refresh control circuit 10 for refresh the memory cell by applying a positive and negative electric field for causing the states of memory cell array 1 to transit at least one completed, figure 1; also see column 9, lines 18-23**).

With respect to claim 4, Takata et al discloses in figure 6, the refresh complete circuit provides a signal (**refresh signal DQ for access counter 10a when data is HIGH and access counter 10b when data is LOW, figure 6**) indicating when the refresh operation is complete (**see column 12, lines 13-21**).

Regarding claim 5, Takata et al disclose in figure 1, a memory refresh circuit comprising:

a memory array (**memory array 1, figure 1**);

a control circuit (**main control circuit 9, figure 1**) for conducting a memory refresh operation (**by using refresh control circuit 10, figure 1**) for monitoring a memory device (**memory array 1, figure 1**) and for indicating when the refresh operation is complete (**the refresh control circuit 10 for refresh the memory cell by applying a positive and negative electric field for causing the states of memory cell array 1 to transit at least one completed; also see column 9, lines 18-23**) based on the monitoring of the memory device (**main control circuit 9 coupled to memory array 1 through refresh control circuit 10 for refreshing individual memory cells MC array 1; also see column 9, lines 14-27**).

With respect to claim 6, Takata et al discloses in figures 1 and 6, the refresh circuit (**refresh circuit 10, figure 1**) includes a refresh counter (**refresh counter 10a, 10b, figure 6; also see column 11, lines 24-27**).

With respect to claim 7, Takata et al discloses in figures 1 and 6, the refresh circuit (**refresh circuit 10, figure 1**) comprises a refresh complete circuit (**the refresh circuit 10 including a first counter 10a corresponding to the memory cell MC when data DQ access at the HIGH level and a second counter 10b corresponding to the memory cell MC when data DQ access at the LOW level in figure 6; also see**

column 12, lines 13-21) for indicating when the refresh operation is complete (**the refresh control circuit 10 operation including positive and negative electric field for causing the states of memory cell array 1 to transit at least one completed round; also see column 9, lines 18-23**).

With respect to claim 8, Takata et al discloses in figure 6, the refresh complete circuit provides a signal (**refresh signal DQ for access counter 10a when data is HIGH and access counter 10b when data is LOW, figure 6**) indicating when the refresh operation is complete (**see column 12, lines 13-21**).

Regarding claim 62, Takata et al discloses in figure 1, an integrated circuit comprising:

a memory device comprising a memory array (**memory array 1, figure 1**);

a control circuit (**main control circuit 9, figure 1**) for conducting a memory refresh operation (**by using refresh control circuit 10, figure 1**) for monitoring a memory device (**memory array 1, figure 1**) and for indicating when the refresh operation is complete (**the refresh control circuit 10 for refresh the memory cell by applying a positive and negative electric field for causing the states of memory cell array 1 to transit at least one completed; also see column 9, lines 18-23**) based on the monitoring of the memory device (**main control circuit 9 coupled to memory array 1 through refresh control circuit 10 for refreshing individual memory cells MC array 1; also see column 9, lines 14-27**).

With respect to claim 63, Takata et al discloses in figures 1 and 6, the refresh circuit (**refresh circuit 10, figure 1**) includes a refresh counter (**refresh counter 10a, 10b, figure 6; also see column 11, lines 24-27**).

With respect to claim 64, Takata et al discloses in figures 1 and 6, the refresh circuit (**refresh circuit 10, figure 1**) comprises a refresh complete circuit (**the refresh circuit 10 including a first counter 10a corresponding to the memory cell MC when data DQ access at the HIGH level and a second counter 10b corresponding to the memory cell MC when data DQ access at the LOW level in figure 6; also see column 12, lines 13-21**) for indicating when the refresh operation is complete (**the refresh control circuit 10 operation including positive and negative electric field for causing the states of memory cell array 1 to transit at least one completed round; also see column 9, lines 18-23**).

With respect to claim 65, Takata et al discloses in figure 1, the refresh complete circuit (**refresh circuit 10, figure 1**) provides a signal (**refresh signal DQ for access counter 10a when data is HIGH and access counter 10b when data is LOW, figure 6**) indicating when the refresh operation is complete (**see column 12, lines 13-21**).

Regarding claim 74, Takata et al discloses in figure 1, a processor system comprising a processor and a memory device comprising:

a memory array (**memory array, 1, figure 1**);

a control circuit (**main control circuit 9, figure 1**) for conducting a memory refresh operation (**by using refresh control circuit 10, figure 1**) for monitoring a memory device (**memory array 1, figure 1**) and for indicating when the refresh operation is complete (**the refresh control circuit 10 for refresh the memory cell by applying a positive and negative electric field for causing the states of memory cell array 1 to transit at least one completed round; also see column 9, lines 18-23**) based on the monitoring of the memory device (**main control circuit 9 coupled to memory array 1 through refresh control circuit 10 for refreshing individual memory cells MC array 1; also see column 9, lines 14-27**).

With respect to claim 75, Takata et al discloses in figures 1 and 6, the refresh circuit (**refresh circuit 10, figure 1**) includes a refresh counter (**refresh counter 10a, 10b, figure 6, see column 11, lines 24-27**).

With respect to claim 76, Takata et al discloses in figures 1 and 6, the refresh circuit (**refresh circuit 10, figure 1**) comprises a refresh complete circuit (**the refresh circuit 10 including a first counter 10a corresponding to the memory cell MC when data DQ access at the HIGH level and a second counter 10b corresponding to the memory cell MC when data DQ access at the LOW level in figure 6; also see column 12, lines 13-21**) for indicating when the refresh operation is complete (**the refresh control circuit 10 operation including positive and negative electric field**

for causing the states of memory cell array 1 to transit at least one completed round; also see column 9, lines 18-23).

With respect to claim 77, Takata et al discloses in figure 6, the refresh complete circuit (**refresh circuit 10, figure 1**) provides a signal (**refresh signal DQ for access counter 10a when data is HIGH and access counter 10b when data is LOW, figure 6**) indicating when the refresh operation is complete (**see column 9, lines 13-21**).

Allowable Subject Matter

5. Claims 9-11, 66-68 and 78-80 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 9-11, 66-68 and 78-80, the prior art of record do not disclose or suggest a memory device including the control logic circuit providing a first control signal to the refresh circuit and second control signal to the control logic circuit.

6. Claims 12-61, 69-73 and 81-85 are allowed.

The following is an examiner's statement of reasons for allowance:

There is no teaching or suggestion in the prior art to: "a combining circuit for combining the refresh completed signals from the memory device to obtain a combined

refresh complete signal" as claimed in the independent claims 12 and 24. Claims 13-23 and 25-34 are also allowed because of their dependency claims 12 and 24; or

"a temperature integration circuit for incorporating temperature into a refresh operation" as claimed in the independent claims 35 and 42. Claims 36-41 and 43-44 are also allowed because of their dependency claims 35 and 42; or

"a refresh circuitry is adapted to initiate the refresh operation partially in response to the environmental condition sense by the sensor which is indicate when the refresh operation is complete" as claimed in the independent claims 45, 69 and 81. Claims 46-49, 70-73 and 82-85 are also allowed because of their dependency claims 45, 69 and 81.

"a refresh completed signal when the burst self-refresh operation has been completed" as claimed in the independent claim 50. Claims 51-60 are also allowed because of their dependency claim 50; or

"a refresh complete signal form each memory device in the subset when the memory device complete the refresh operation" as claimed in the independent claim 61.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Pho M. Luu whose telephone number is 571.272.1876. The examiner can normally be reached on M-F 8:00AM – 5:00PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Richard Elms, can be reached on 571.272.1869. The official fax number for

the organization where this application or proceeding is assigned is 703.872.9306 for all official communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PML
24 March 2006

4/7/06

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